WJEC 2014 Online Exam Review

GCE Electronics ET1 1141-01

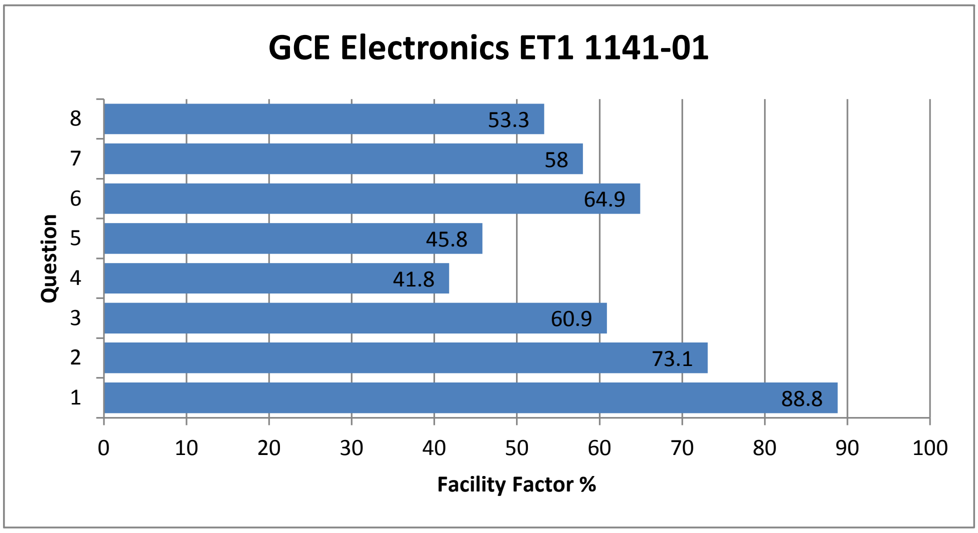
All Candidates' performance across questions

Question Title	*N*	*Mean*	*S D*	*Max Mark*	*F F*	*Attempt %*
1	817	7.1	1.5	8	88.8	99.9
2	812	4.4	2.1	6	73.1	99.3
3	816	5.5	2.4	9	60.9	99.8
4	816	2.9	2.3	7	41.8	99.8
5	813	2.8	2	6	45.8	99.4
6	810	3.2	1.5	5	64.9	99
7	813	4.1	2.2	7	58	99.4
8	803	6.4	3.7	12	53.3	98.2

3

4

8



Examiner only

3. *(a)* Simplify the following expressions, showing your working where appropriate.

(i) $\overline{A}.1$ = ... [1]

(ii) $(B + \overline{A}).(\overline{B} + A)$ = ...

.... [2]

(b) A different logic system produced the Karnaugh map shown below.

DC \ BA	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	1
10	0	0	1	1

Give the simplest Boolean expression for the output Q of this logic system.
Show any groups that you create on the map. [3]

....

....

....

(c) Apply DeMorgan's theorem to the following expression **and** simplify the result.
All steps of the simplification must be shown. [3]

$$Q = \overline{(\overline{A}.\overline{B}).(A + \overline{B})}$$

....

....

....

....

....

1141
010007

Examiner only

3. *(a)* Simplify the following expressions, showing your working where appropriate.

(i) $\bar{A}.1$ = A [1]

(ii) $(B + \bar{A}).(\bar{B} + A)$ = $B+\bar{A} . \bar{B}+A = 0$

[2]

(b) A different logic system produced the Karnaugh map shown below.

DC \ BA	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	1
10	0	0	1	1

Give the simplest Boolean expression for the output Q of this logic system.
Show any groups that you create on the map. [3]

$C.\bar{B} + \bar{C}.B + D.B.\bar{A}$

(c) Apply DeMorgan's theorem to the following expression **and** simplify the result.
All steps of the simplification must be shown. [3]

$$Q = \overline{(\bar{A}.\bar{B}).(A + \bar{B})}$$

$\overline{(\bar{A}.\bar{B})} + \overline{(A+\bar{B})}$ $\quad (\bar{\bar{A}}+\bar{\bar{B}}) + (\bar{A}.\bar{\bar{B}})$

$\bar{A}+\bar{B}+A.\bar{B} \quad = \bar{B}$

1141 010007

Examiner only

3. *(a)* Simplify the following expressions, showing your working where appropriate.

(i) $\bar{A}.1$ = A [1]

(ii) $(B + \bar{A}).(\bar{B} + A)$ = $B + \bar{A} . \bar{B} + A \quad = 0$

[2]

(b) A different logic system produced the Karnaugh map shown below.

DC \ BA	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	1
10	0	0	1	1

Give the simplest Boolean expression for the output Q of this logic system.
Show any groups that you create on the map. [3]

$C . \bar{B} + \bar{C} . B + D . B . \bar{A}$

(c) Apply DeMorgan's theorem to the following expression **and** simplify the result.
All steps of the simplification must be shown. [3]

$$Q = \overline{(\bar{A}.\bar{B}).(A + \bar{B})}$$

$\overline{(\bar{A} . \bar{B})} + \overline{(A + \bar{B})} \qquad (\bar{\bar{A}} + \bar{\bar{B}}) + (\bar{A} . \bar{\bar{B}})$

$\bar{A} + \bar{B} + A . \bar{B} \qquad = \bar{B}$

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Examiner only

3. *(a)* Simplify the following expressions, showing your working where appropriate.

(i) $\bar{A}.1$ = $\bar{A}$ [1]

(ii) $(B+\bar{A}).(\bar{B}+A)$ = $\bar{B}.\bar{A}$

[2]

(b) A different logic system produced the Karnaugh map shown below.

DC \ BA	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	1
10	0	0	1	1

Give the simplest Boolean expression for the output Q of this logic system.
Show any groups that you create on the map. [3]

$Q = C.\bar{B} + B.\bar{C} + D.\bar{C}.B$

(c) Apply DeMorgan's theorem to the following expression **and** simplify the result.
All steps of the simplification must be shown. [3]

$$Q = \overline{(\bar{A}.\bar{B}).(A+\bar{B})}$$

$Q = (\overline{\bar{A}.\bar{B}}).(\overline{A+\bar{B}})$

$Q = (A.B).(\bar{A}+B)$

$Q = \bar{A}.B$

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Examiner only

3. *(a)* Simplify the following expressions, showing your working where appropriate.

(i) $\overline{A}.1$ = $\overline{A}$ [1] 1

(ii) $(B + \overline{A}).(\overline{B} + A)$ = $\overline{B}.\overline{A}$ [2] 0

(b) A different logic system produced the Karnaugh map shown below.

DC \ BA	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	1
10	0	0	1	1

Give the simplest Boolean expression for the output Q of this logic system.
Show any groups that you create on the map. [3] 2

$Q = C.\overline{B} + B.\overline{C} + D.\overline{C}.B$

(c) Apply DeMorgan's theorem to the following expression **and** simplify the result.
All steps of the simplification must be shown. [3] 0

$$Q = \overline{(\overline{A}.\overline{B})}.(\overline{A + \overline{B}})$$

$Q = (\overline{\overline{A}.\overline{B}}).(\overline{A + \overline{B}})$

$Q = (A + B).(\overline{A} . B)$

$Q = \overline{A}.B$

3

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Examiner only

3. *(a)* Simplify the following expressions, showing your working where appropriate.

(i) $\bar{A}.1$ = 1 [1]

(ii) $(B + \bar{A}).(\bar{B} + A)$ = ~~A + B~~ A + B

[2]

(b) A different logic system produced the Karnaugh map shown below.

DC \ BA	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	1
10	0	0	1	1

Give the simplest Boolean expression for the output Q of this logic system.
Show any groups that you create on the map. [3]

$C.\bar{B} + \bar{C}.B$

(c) Apply DeMorgan's theorem to the following expression **and** simplify the result.
All steps of the simplification must be shown. [3]

$$Q = (\overline{\bar{A}.\bar{B}})(\overline{A + \bar{B}})$$

$\overline{\bar{A}.\bar{B}} + \overline{A + \bar{B}}$

$\bar{\bar{A}} + \bar{\bar{B}} + \overline{A + \bar{B}}$ $A + B + \bar{A}.B$

$A + B + \overline{A + \bar{\bar{B}}}$ $= B$

$A + B + \bar{A}.B$

1141
010007

Examiner only

3. *(a)* Simplify the following expressions, showing your working where appropriate.

(i) $\bar{A}.1$ = 1 [1]

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[2]

(b) A different logic system produced the Karnaugh map shown below.

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$$Q = \overline{(\bar{A}.\bar{B})(\bar{A + \bar{B}})}$$

$\overline{\bar{A}.\bar{B}} + \overline{\overline{A + \bar{B}}}$

$\bar{\bar{A}} + \bar{\bar{B}} + \overline{\overline{A + \bar{B}}}$ $\qquad A + B + \bar{A}.B$

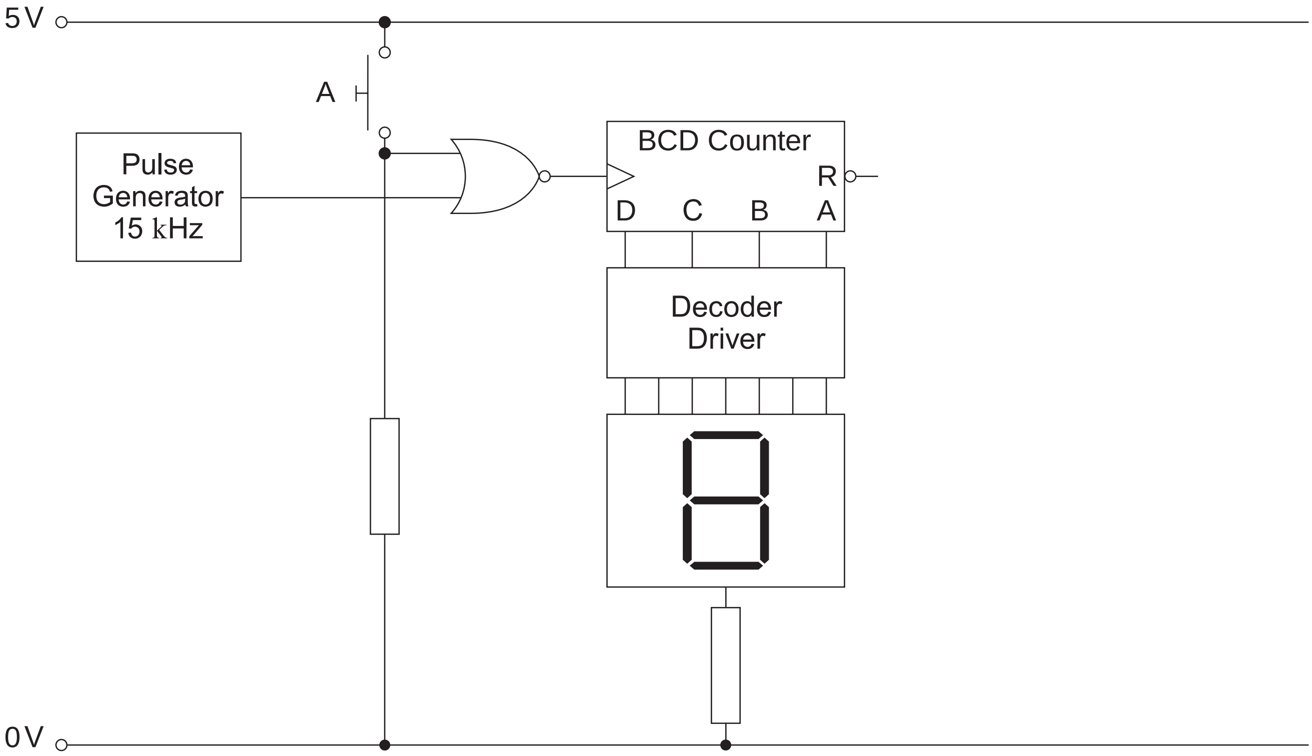
$A + B + \overline{A + \bar{B}}$ $\qquad = B$

$A + B + \bar{A}.B$

1141 010007

Examiner only

4. The incomplete circuit diagram shows a simple random number generator.



(a) (i) What does the circle (○) on the reset connection indicate? [1]

....

(ii) **Complete** the circuit diagram by adding a logic gate and suitable connections so that the largest number displayed is 5. [3]

(b) Describe, in detail, what happens to the display when:

(i) switch A is open; [1]

....

....

(ii) switch A is pressed and held closed. [1]

....

....

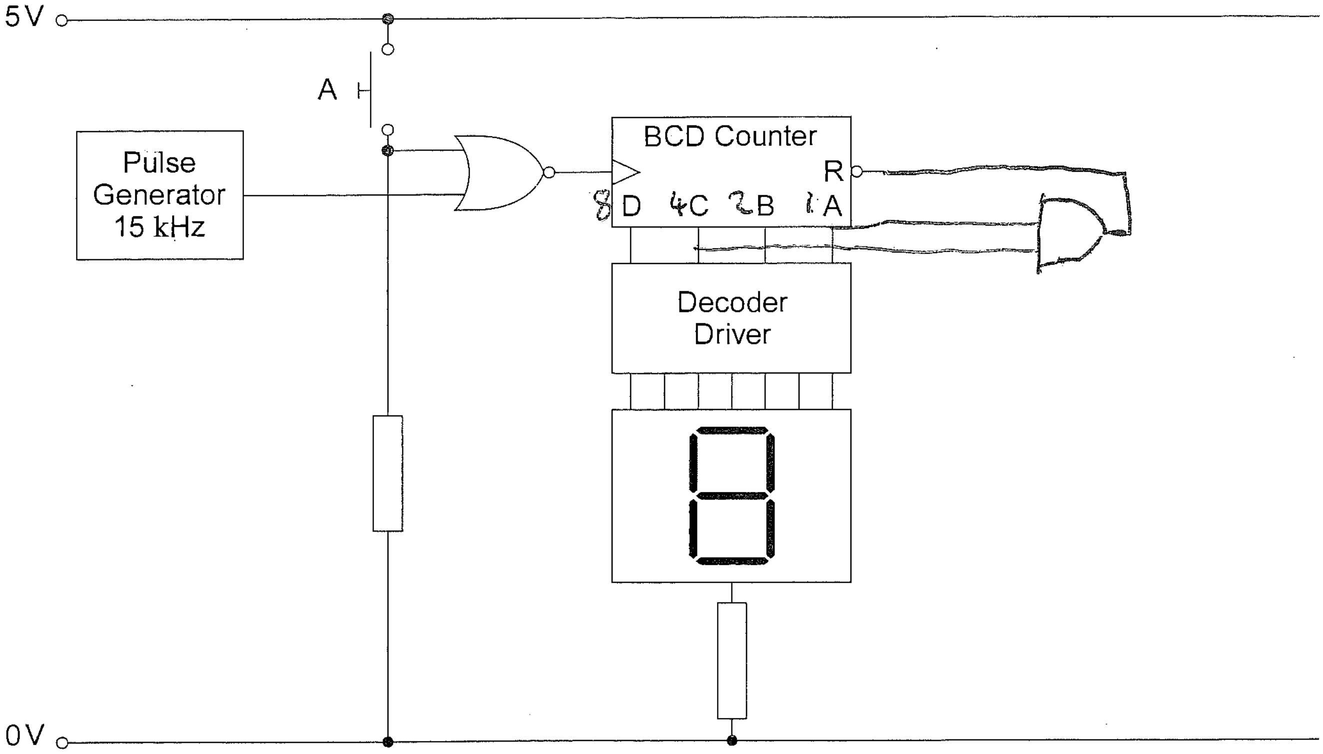
(c) Explain why a 15 kHz astable is suitable for this application. [1]

....

....

Examiner only

4. The incomplete circuit diagram shows a simple random number generator.



(a) (i) What does the circle (o) on the reset connection indicate? [1]

Inverted

(ii) **Complete** the circuit diagram by adding a logic gate and suitable connections so that the largest number displayed is 5. [3]

(b) Describe, in detail, what happens to the display when:

(i) switch A is open; [1]

Nothing will happen as there is no connection to 5V

(ii) switch A is pressed and held closed. [1]

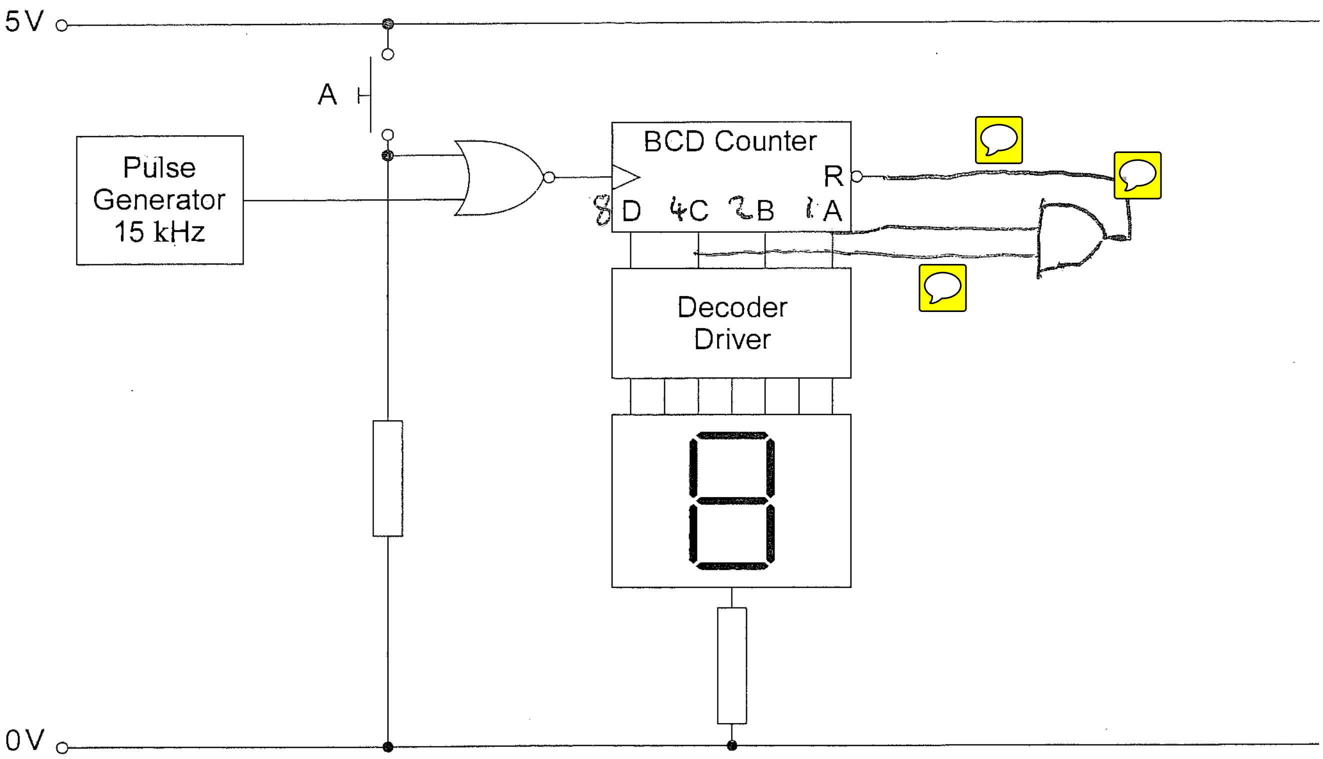
The display will flash on and off each time with a different number

(c) Explain why a 15 kHz astable is suitable for this application. [1]

will make it flash on long enough to be visible to the human eye

Examiner only

4. The incomplete circuit diagram shows a simple random number generator.



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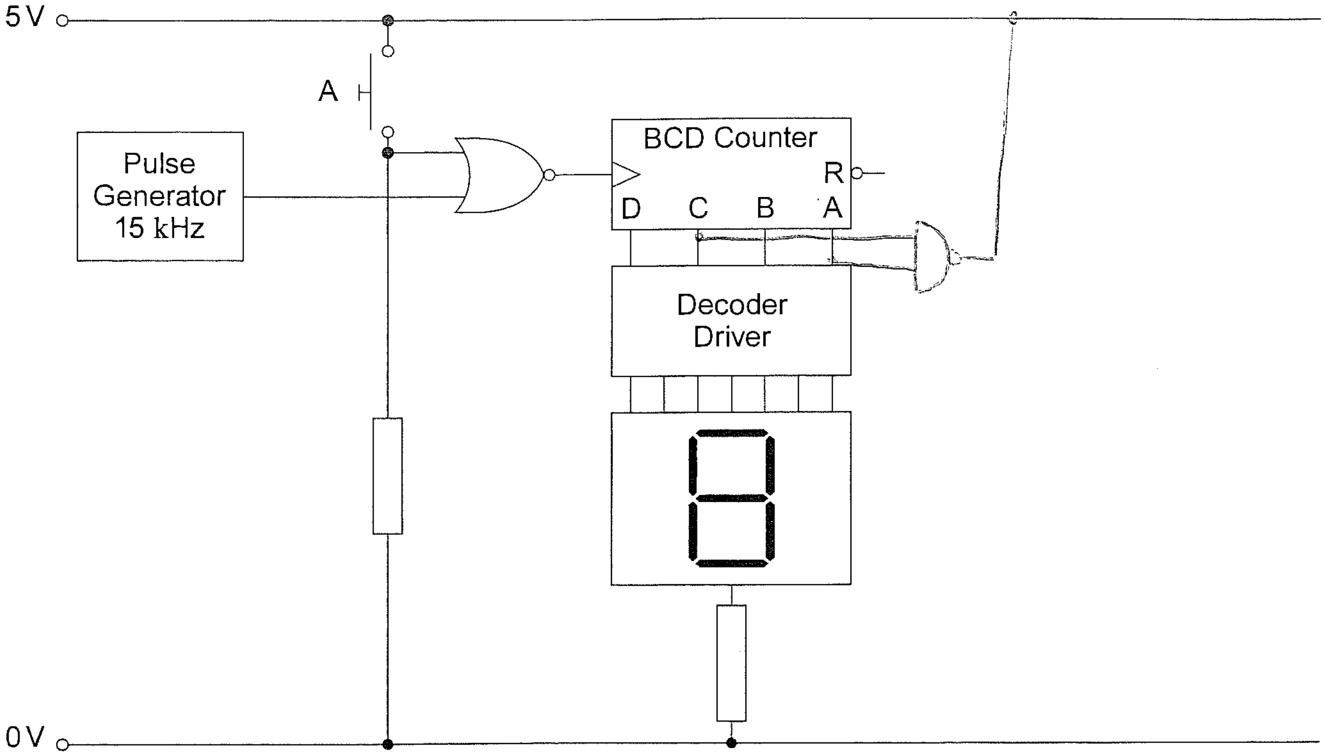


(a) (i) What does the circle (o) on the reset connection indicate? [1]

Means it is Logic 0 activated

(ii) **Complete** the circuit diagram by adding a logic gate and suitable connections so that the largest number displayed is 5. [3]

(b) Describe, in detail, what happens to the display when:

(i) switch A is open; [1]

the pulse generator generates random numbers

(ii) switch A is pressed and held closed. [1]

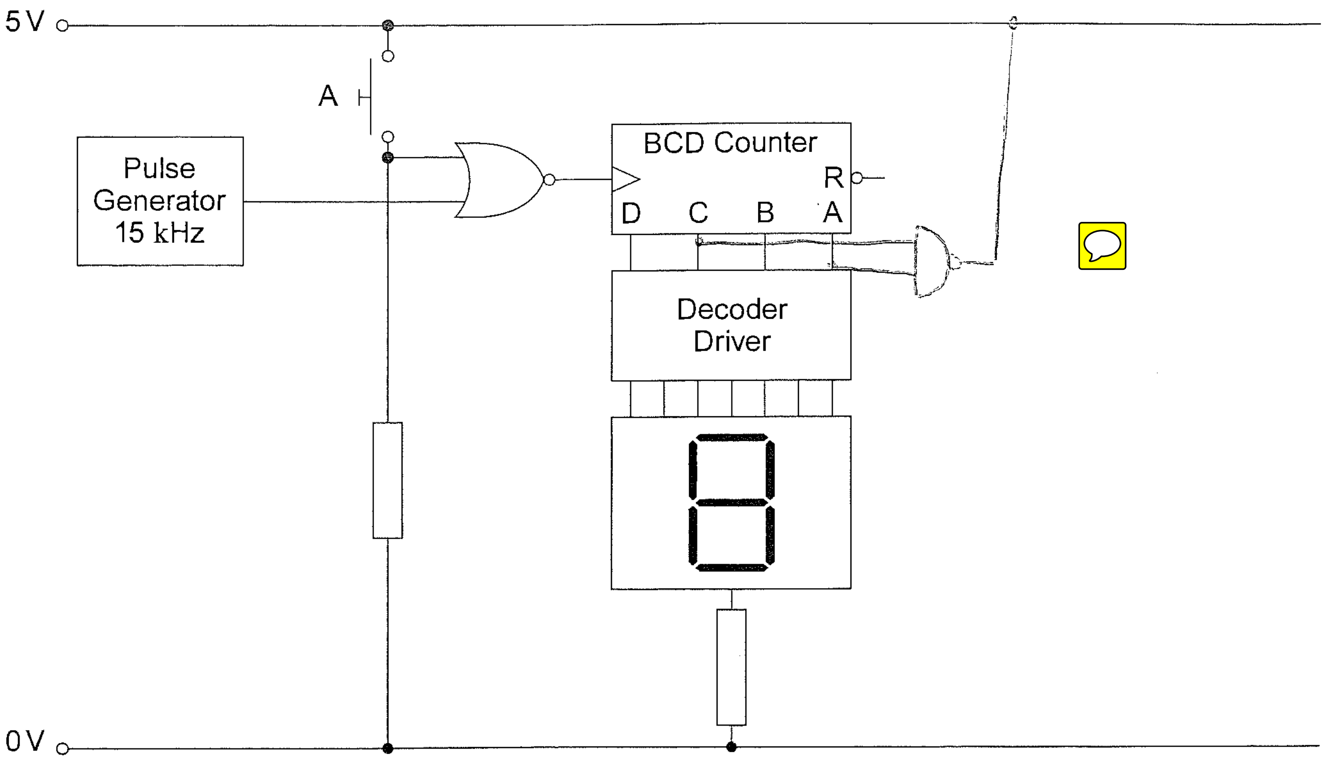
the pulse generator stops and gives out a random number

(c) Explain why a 15 kHz astable is suitable for this application. [1]

Because it generates 15 thousand random numbers per second

Examiner only

4. The incomplete circuit diagram shows a simple random number generator.



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the pulse generator generates random numbers

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Examiner only

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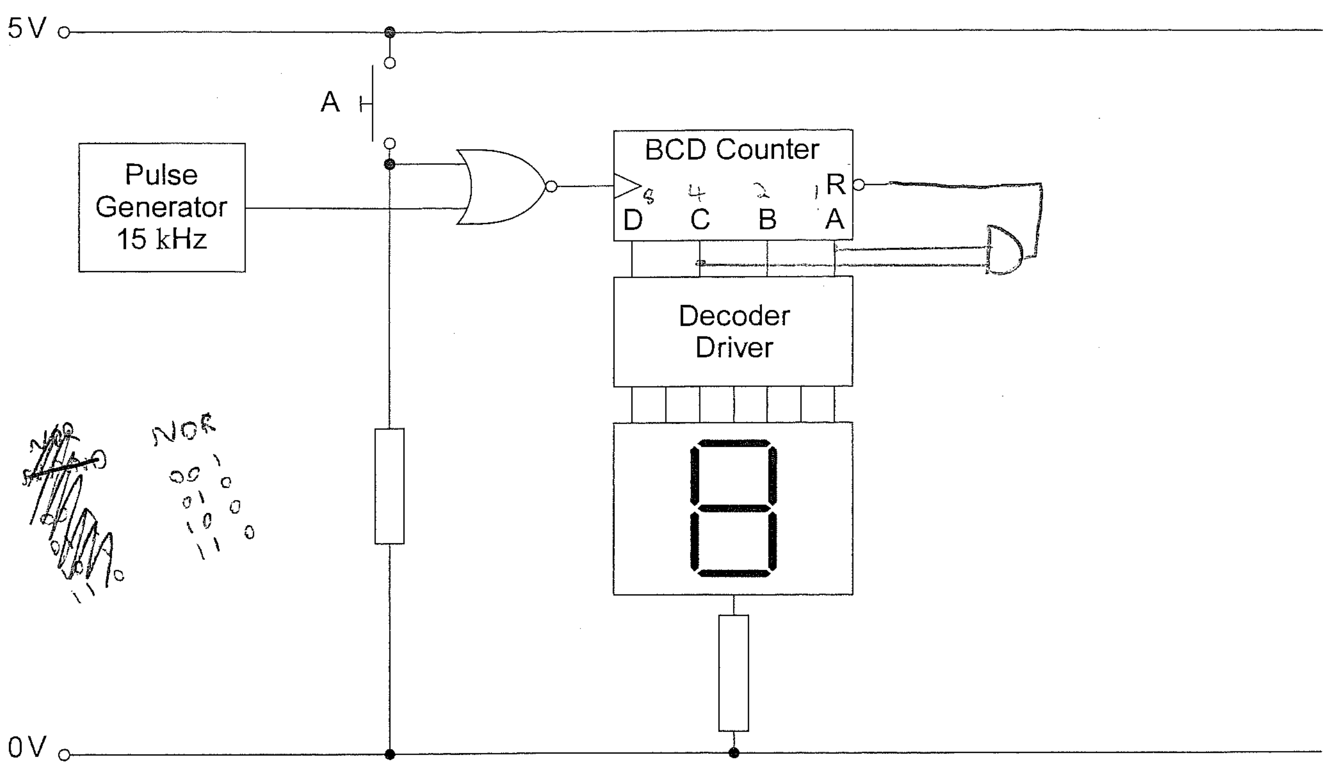

(a) (i) What does the circle (○) on the reset connection indicate? [1]

It resets at a logic 0

(ii) **Complete** the circuit diagram by adding a logic gate and suitable connections so that the largest number displayed is 5. [3]

(b) Describe, in detail, what happens to the display when:

(i) switch A is open; [1]

it activates the BCD counter Providing a fixed width pulse.

(ii) switch A is pressed and held closed. [1]

Nothing will happen to the display as the NOR gate wont function.

(c) Explain why a 15 kHz astable is suitable for this application. [1]

Because it will turn on and then stay on.

Examiner only

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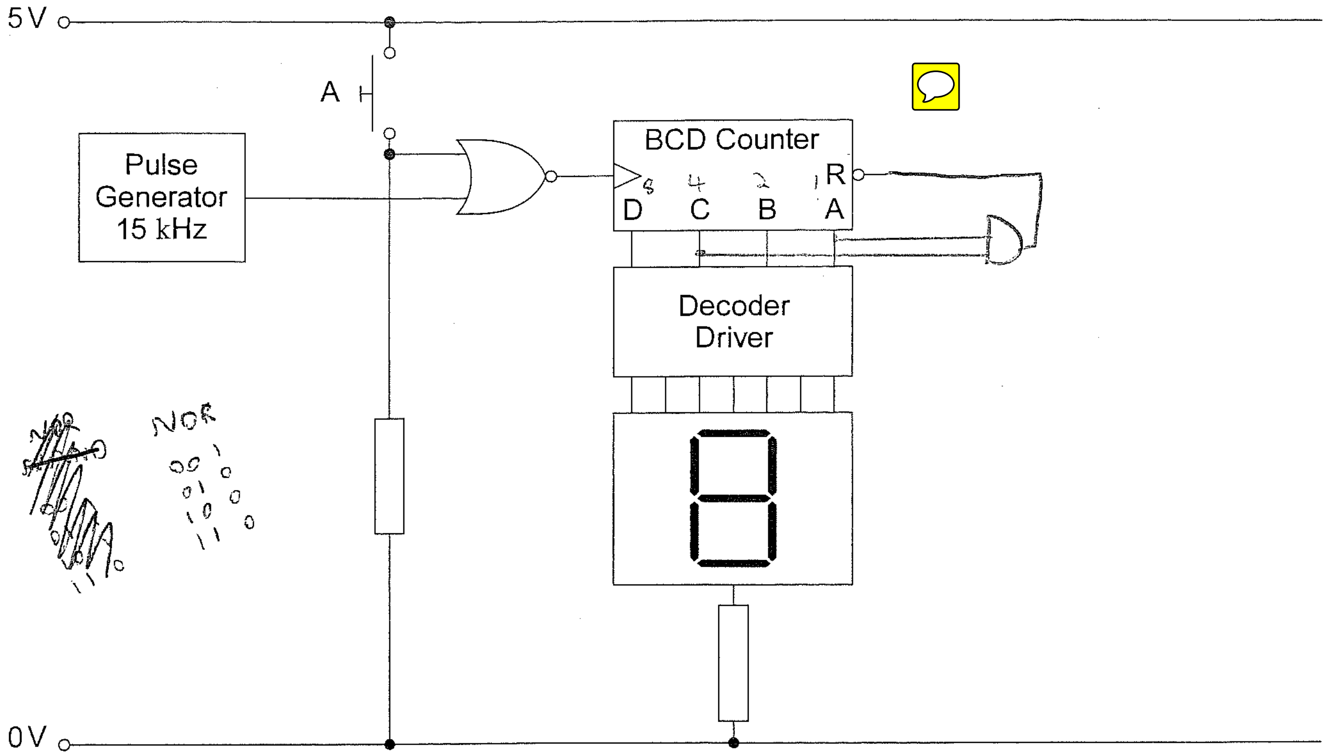

(a) (i) What does the circle (o) on the reset connection indicate? [1]

It resets at a logic 0

(ii) **Complete** the circuit diagram by adding a logic gate and suitable connections so that the largest number displayed is 5. [3]

(b) Describe, in detail, what happens to the display when:

(i) switch A is open; [1]

it activates the BCD counter Providing a fixed width pulse.

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Nothing will happen to the display as the NOR gate wont function.

(c) Explain why a 15 kHz astable is suitable for this application. [1]

Because it will turn on and then stay on.

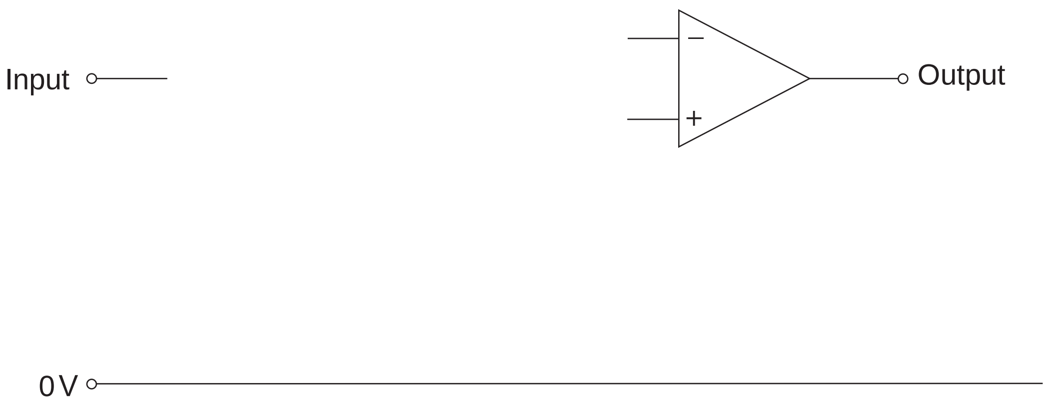
8. A data sheet for an op-amp is given below.

Parameter	**Value**
Open-loop gain	3.0×10^5
Input impedance	$2.0 \times 10^{12} \Omega$
Saturation voltage for a ± 13 V supply	± 12 V
Slew rate	$4.8\ \text{V}\ \mu\text{s}^{-1}$
Gain-bandwidth product	3.6 MHz

The op-amp is powered from a ± 13 V supply.

An amplifier has a **variable** voltage gain. The minimum voltage gain is 0 and the maximum voltage gain is – 60.

(a) Complete the circuit diagram for a voltage amplifier with this specification. [3]



Examiner only

(b) (i) Calculate the **two** resistance values which give a maximum voltage gain of -60. Identify the feedback resistance. [2]

....

....

(ii) What is the input impedance of this voltage amplifier? [1]

....

(c) The voltage gain is adjusted and the output voltage measured to be -9 V when the input voltage is 200 mV. Calculate the new voltage gain. [1]

....

....

(d) The voltage gain is changed to -30. Calculate the maximum bandwidth of the amplifier with this voltage gain. [2]

....

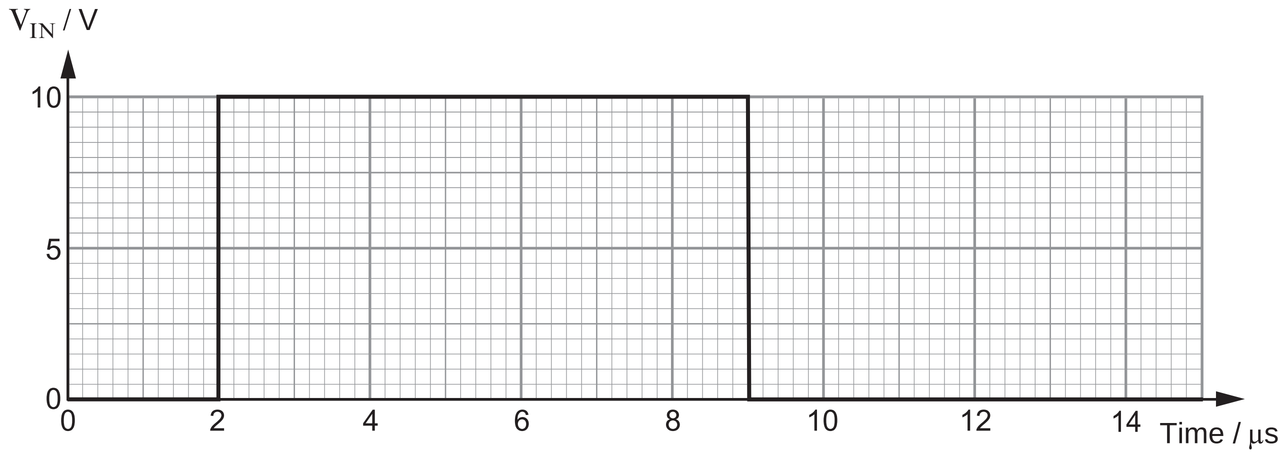
....

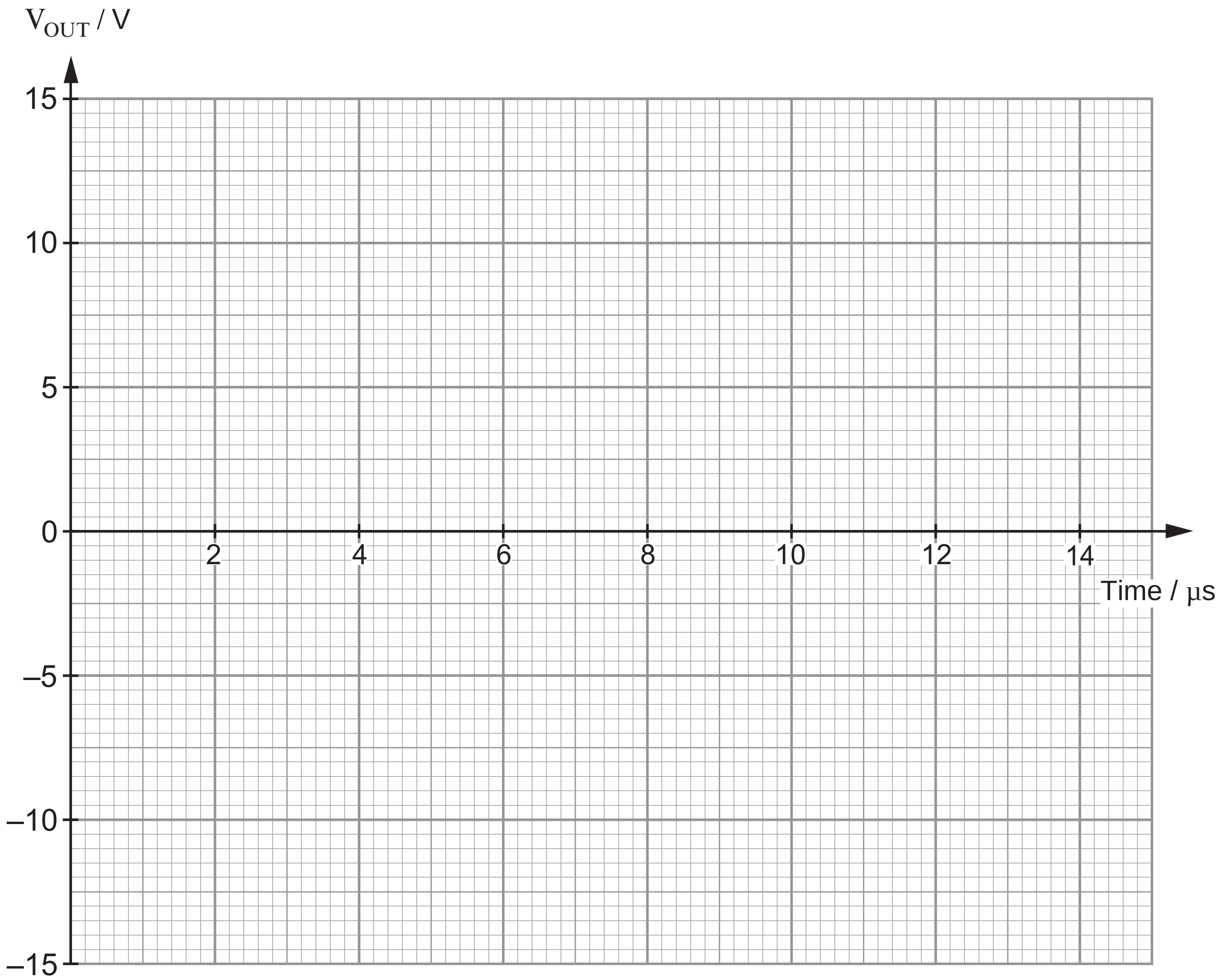
TURN OVER FOR THE REST OF THE QUESTION.

Examiner only

(e) The following signal is applied to the input to illustrate the effect of slew-rate on the output of the voltage amplifier.

Draw the output voltage on the axes below. V_{OUT} **is initially at 0 V**. [3]





END OF PAPER

Examiner only

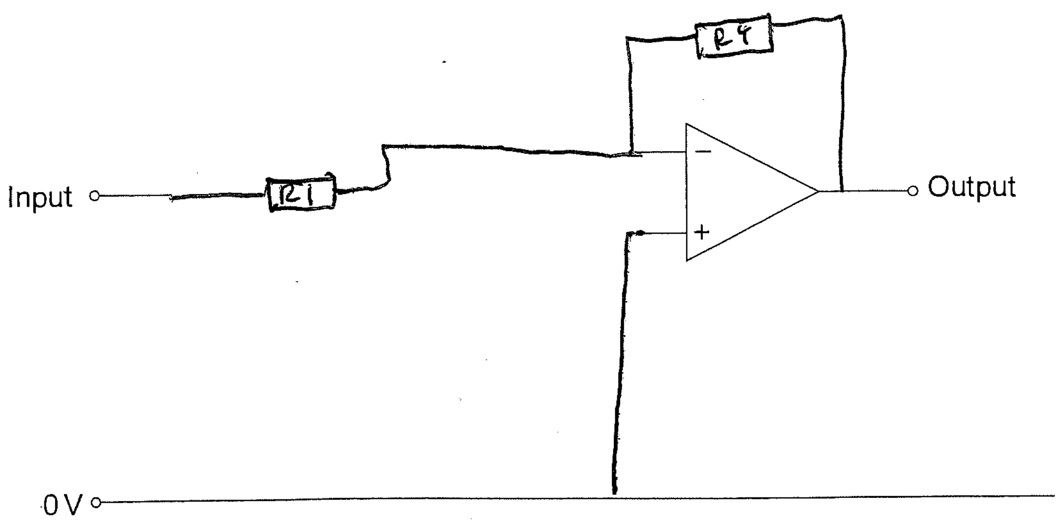
8. A data sheet for an op-amp is given below.

Parameter	**Value**
Open-loop gain	3.0×10^5
Input impedance	$2.0 \times 10^{12}\,\Omega$
Saturation voltage for a ± 13 V supply	± 12 V
Slew rate	$4.8\ \mathrm{V\,\mu s^{-1}}$
Gain-bandwidth product	3.6 MHz

The op-amp is powered from a ± 13 V supply.

An amplifier has a **variable** voltage gain. The minimum voltage gain is 0 and the maximum voltage gain is −60.

(a) Complete the circuit diagram for a voltage amplifier with this specification. [3]



Examiner only

(b) (i) Calculate the **two** resistance values which give a maximum voltage gain of −60. Identify the feedback resistance. [2]

Rf = 59

Ri = 1

(ii) What is the input impedance of this voltage amplifier? [1]

2.0×10^{12}

(c) The voltage gain is adjusted and the output voltage measured to be −9 V when the input voltage is 200 mV. Calculate the new voltage gain. [1]

8.8

(d) The voltage gain is changed to −30. Calculate the maximum bandwidth of the amplifier with this voltage gain. [2]

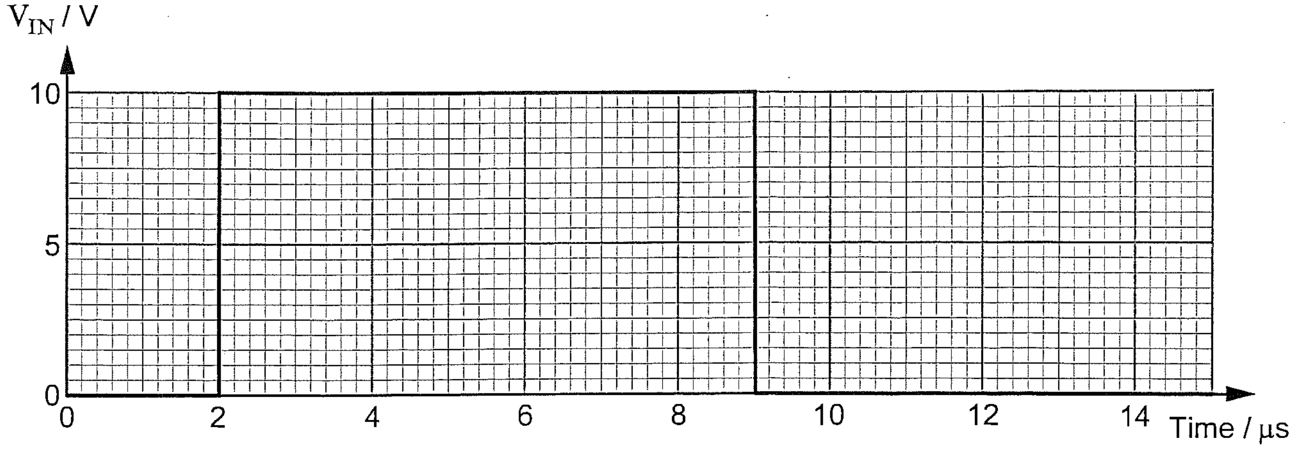
0.2 + 30 = 29.8

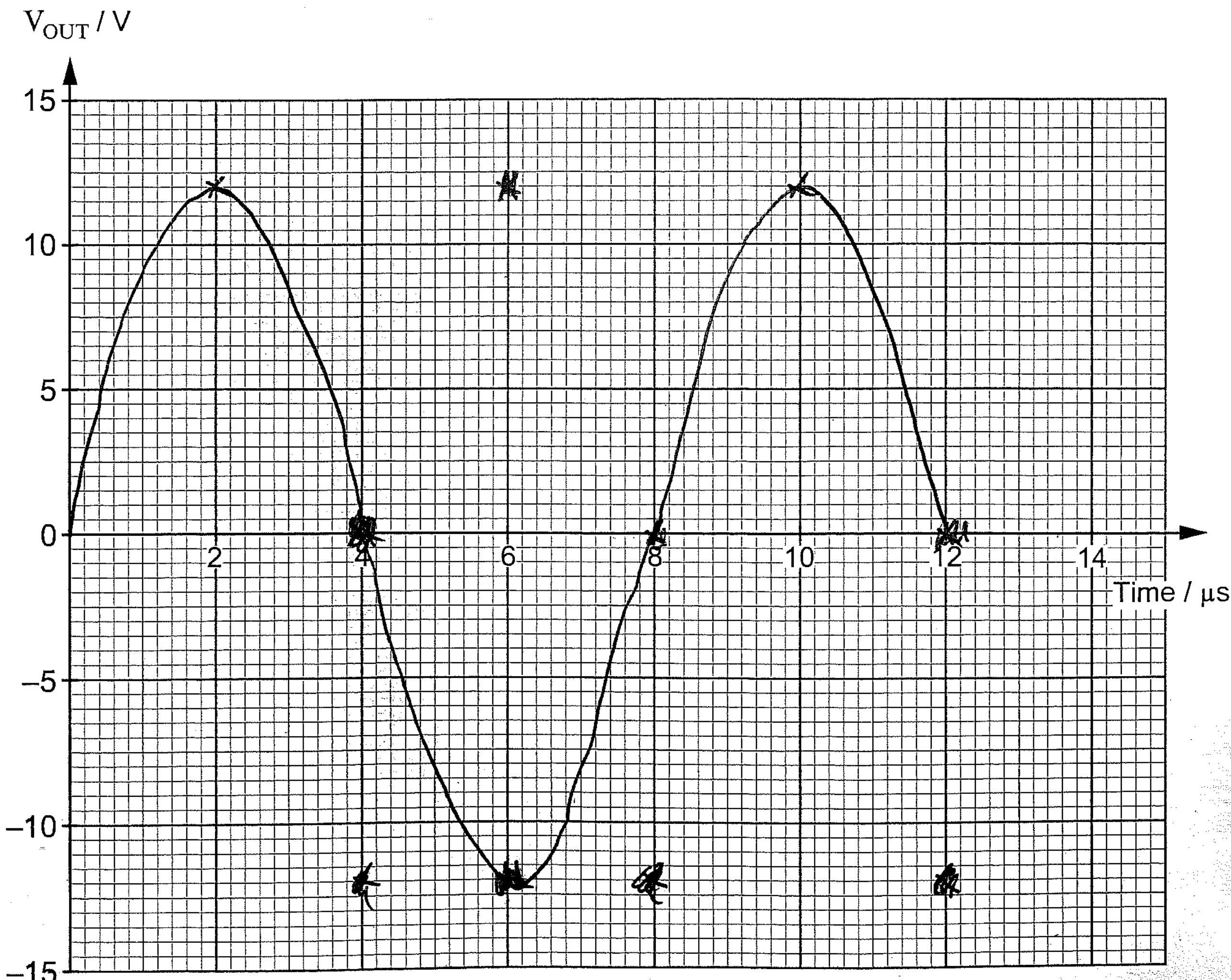
TURN OVER FOR THE REST OF THE QUESTION.

Examiner only

(e) The following signal is applied to the input to illustrate the effect of slew-rate on the output of the voltage amplifier.

Draw the output voltage on the axes below. V_{OUT} **is initially at 0 V.** [3]





END OF PAPER

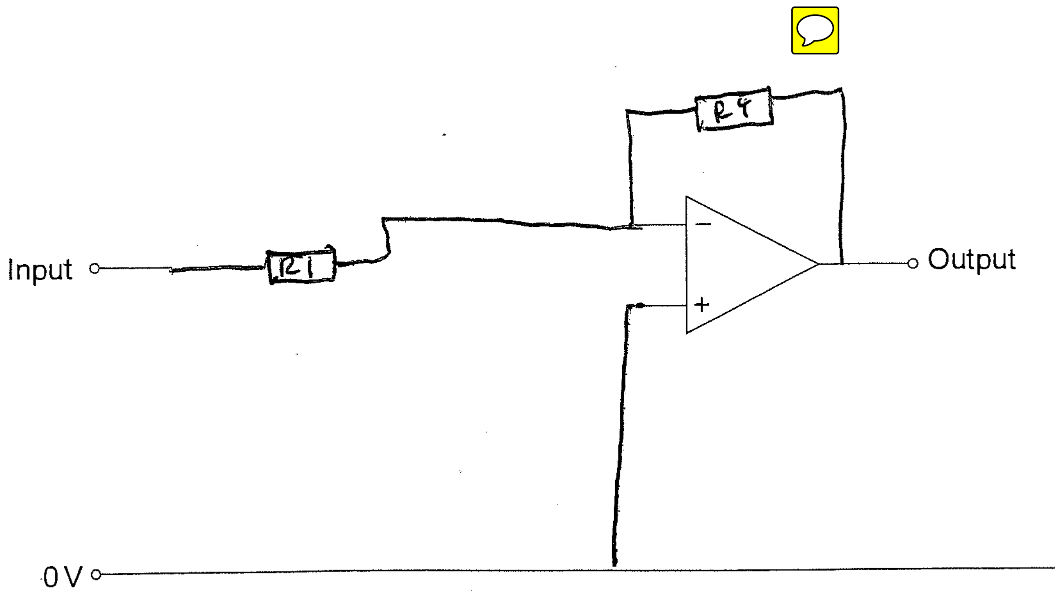
8. A data sheet for an op-amp is given below.

Parameter	**Value**
Open-loop gain	3.0×10^5
Input impedance	$2.0 \times 10^{12}\,\Omega$
Saturation voltage for a ± 13 V supply	± 12 V
Slew rate	$4.8\ \text{V}\ \mu\text{s}^{-1}$
Gain-bandwidth product	3.6 MHz

The op-amp is powered from a ± 13 V supply.

An amplifier has a **variable** voltage gain. The minimum voltage gain is 0 and the maximum voltage gain is −60.

(a) Complete the circuit diagram for a voltage amplifier with this specification. [3]



Examiner only

(b) (i) Calculate the **two** resistance values which give a maximum voltage gain of −60. Identify the feedback resistance. [2]

Rf = 59

Ri = 1

(ii) What is the input impedance of this voltage amplifier? [1]

2.0×10^{12}

(c) The voltage gain is adjusted and the output voltage measured to be −9 V when the input voltage is 200 mV. Calculate the new voltage gain. [1]

8.8

(d) The voltage gain is changed to −30. Calculate the maximum bandwidth of the amplifier with this voltage gain. [2]

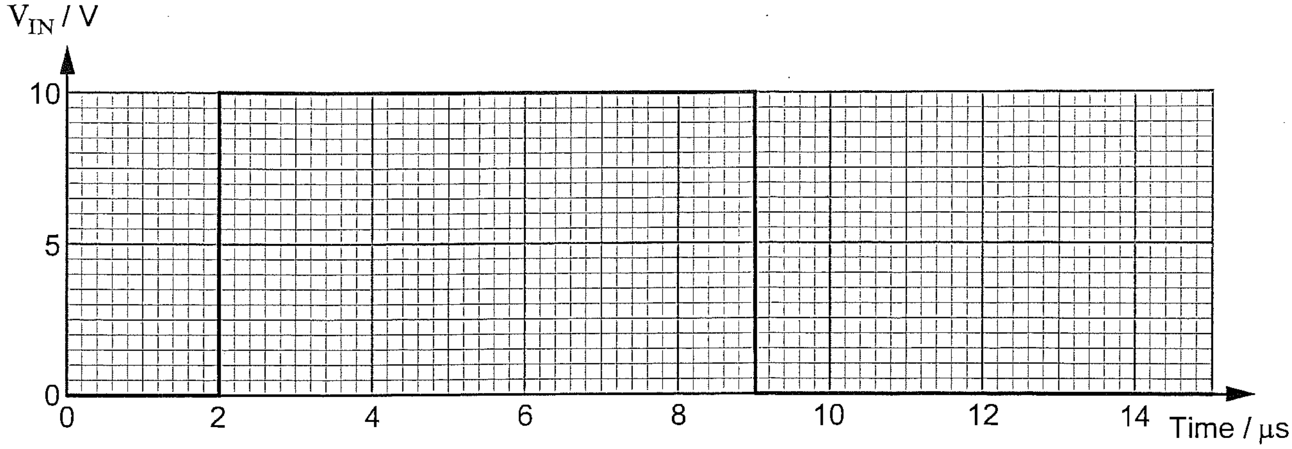
0.2 + ~~29.8~~ 30 = 29.8

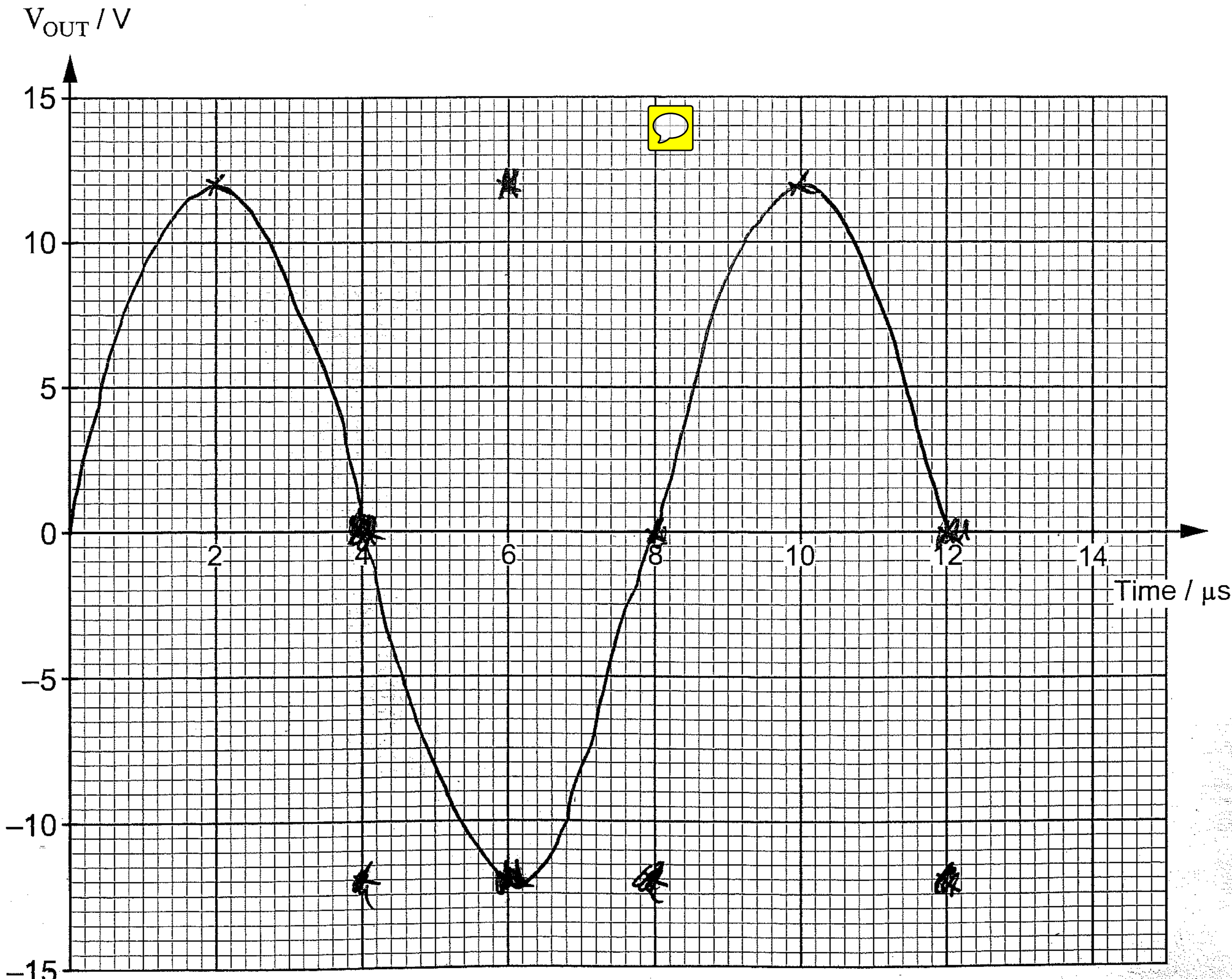
TURN OVER FOR THE REST OF THE QUESTION.

Examiner only

(e) The following signal is applied to the input to illustrate the effect of slew-rate on the output of the voltage amplifier.

Draw the output voltage on the axes below. V_{OUT} **is initially at 0 V.** [3]





END OF PAPER

Examiner only

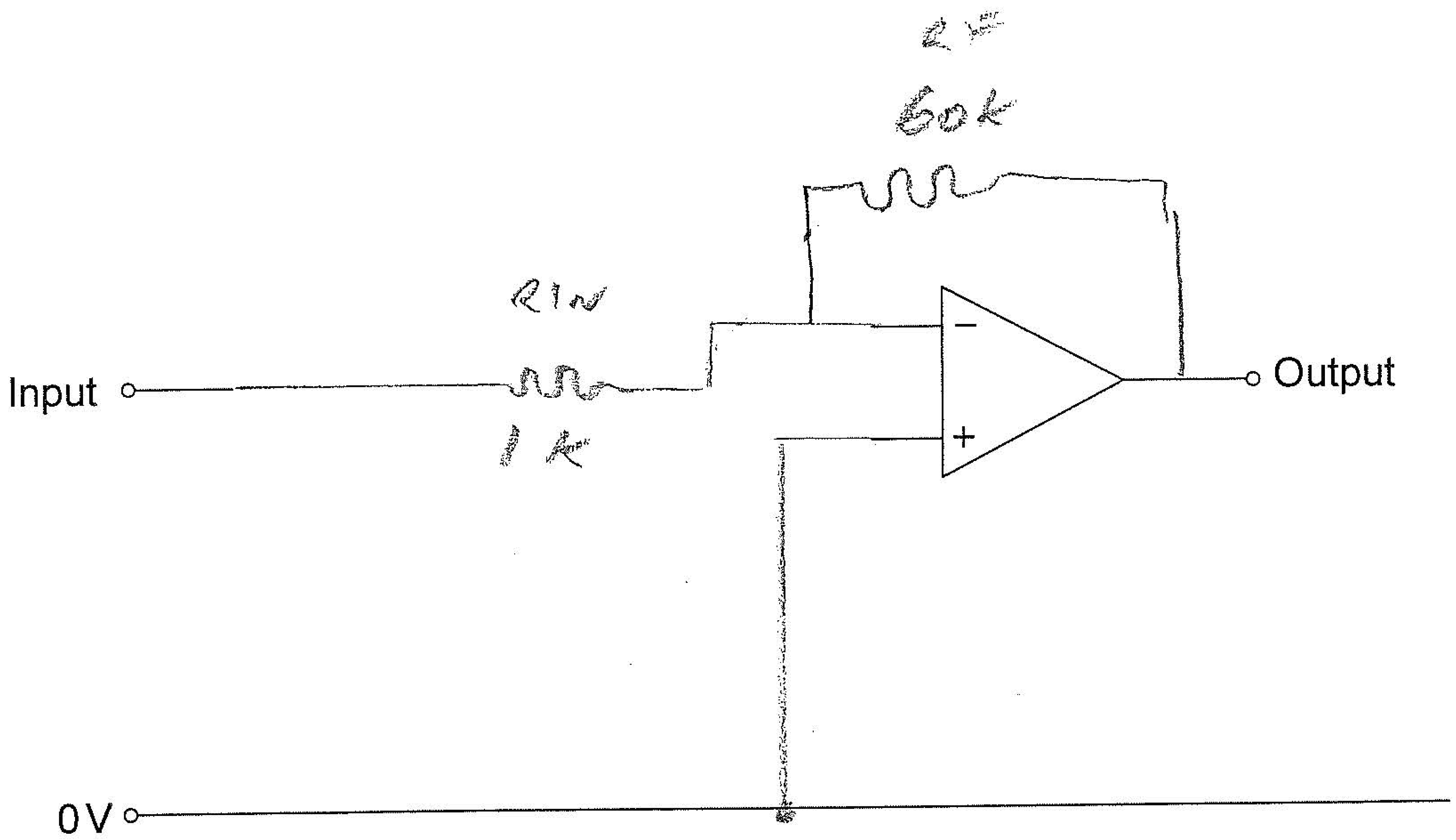
8. A data sheet for an op-amp is given below.

Parameter	**Value**
Open-loop gain	3.0×10^5
Input impedance	$2.0 \times 10^{12} \Omega$
Saturation voltage for a ± 13 V supply	± 12 V
Slew rate	$4.8\ \text{V}\ \mu\text{s}^{-1}$
Gain-bandwidth product	3.6 MHz

The op-amp is powered from a ± 13 V supply.

An amplifier has a **variable** voltage gain. The minimum voltage gain is 0 and the maximum voltage gain is −60.

(a) Complete the circuit diagram for a voltage amplifier with this specification. [3]



Examiner only

(b) (i) Calculate the **two** resistance values which give a maximum voltage gain of −60. Identify the feedback resistance. [2]

RF = 60k   −60/1 = −60

Rin = 1k

(ii) What is the input impedance of this voltage amplifier? [1]

1k (Rin)

(c) The voltage gain is adjusted and the output voltage measured to be −9 V when the input voltage is 200 mV. Calculate the new voltage gain. [1]

−9/200m = −45v

(d) The voltage gain is changed to −30. Calculate the maximum bandwidth of the amplifier with this voltage gain. [2]

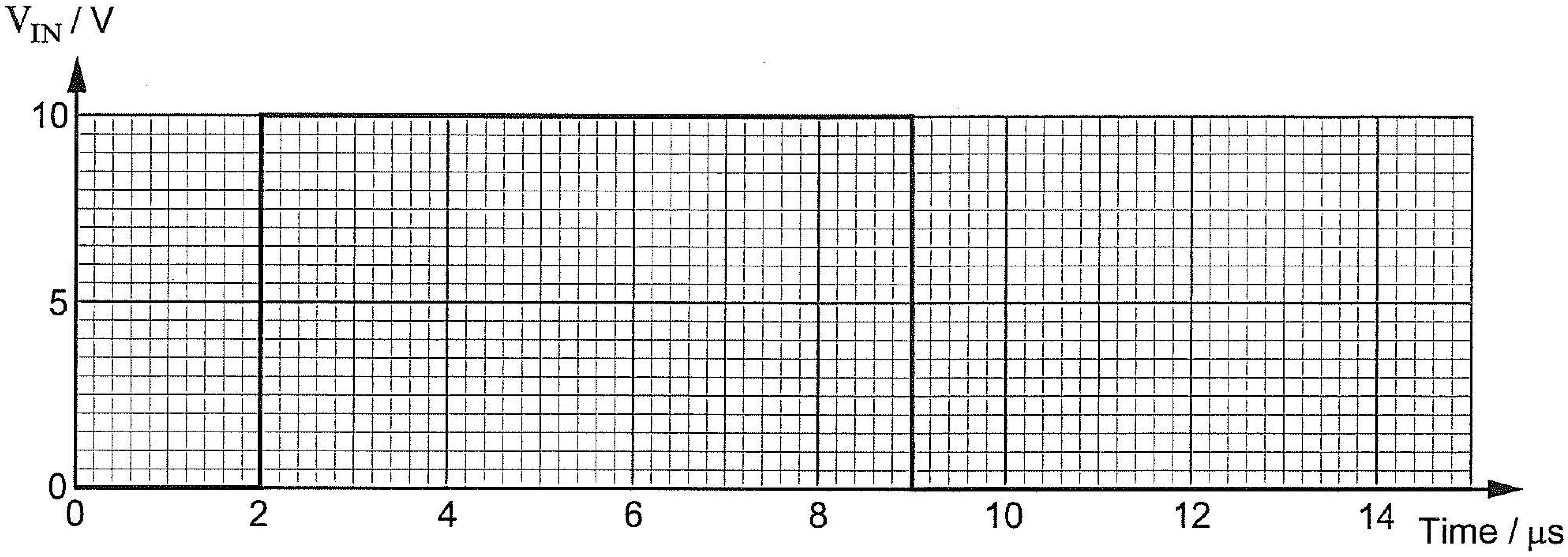
3.6M/30 = 120k Hz

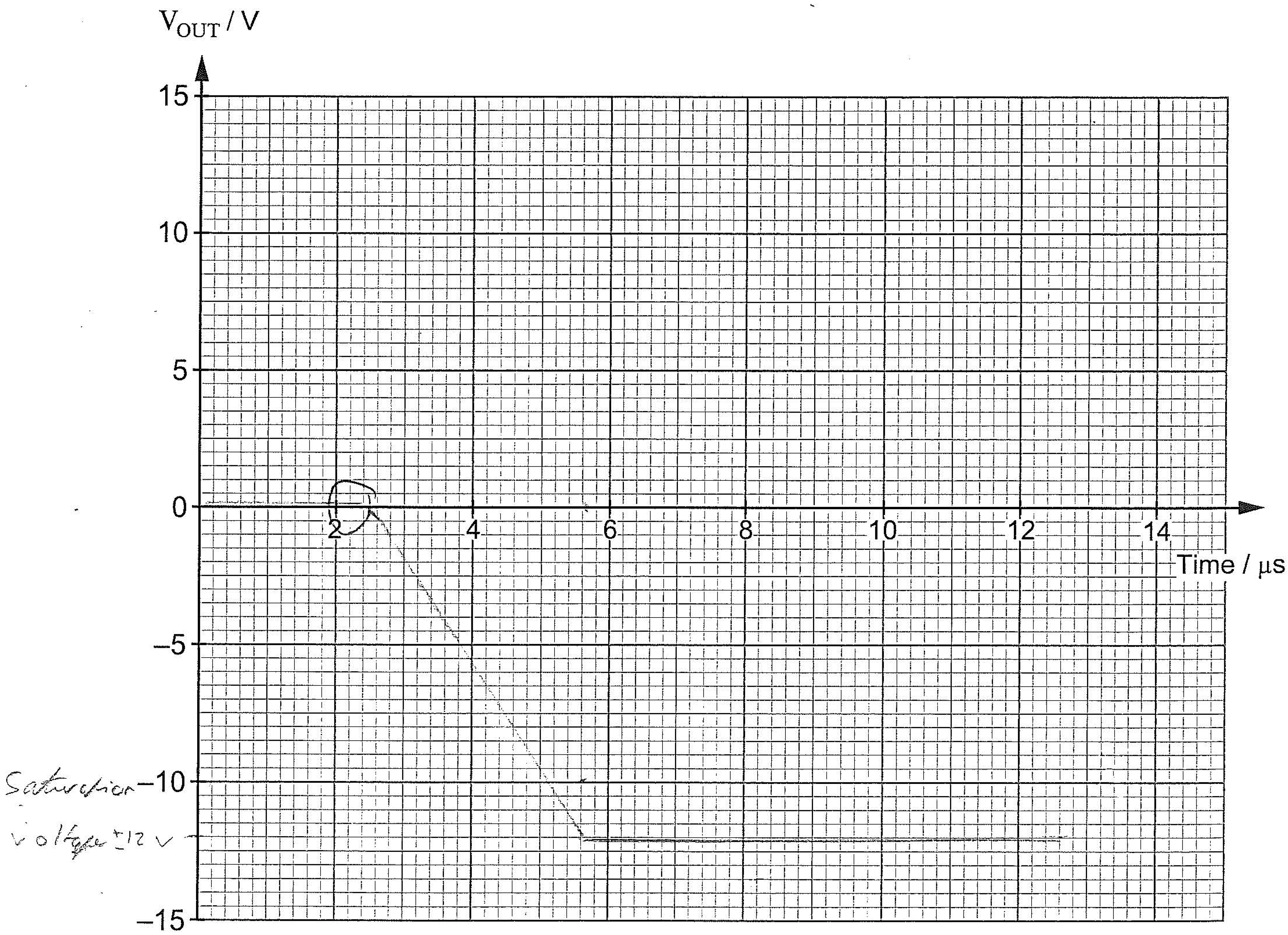
TURN OVER FOR THE REST OF THE QUESTION.

Examiner only

(e) The following signal is applied to the input to illustrate the effect of slew-rate on the output of the voltage amplifier.

Draw the output voltage on the axes below. V_{OUT} **is initially at 0 V**. [3]





END OF PAPER

Examiner only

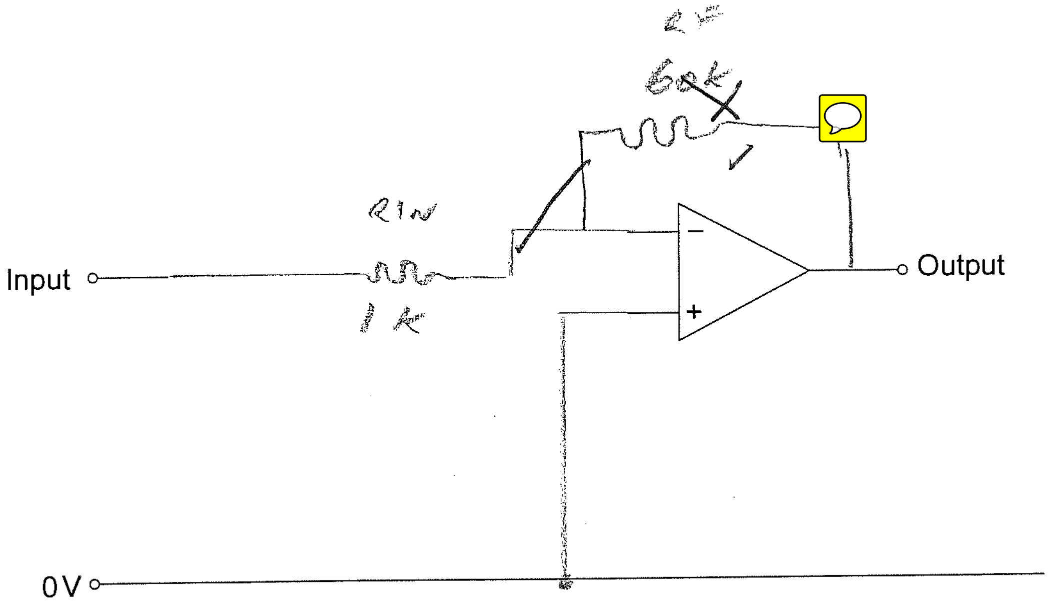
8. A data sheet for an op-amp is given below.

Parameter	**Value**
Open-loop gain	3.0×10^5
Input impedance	$2.0 \times 10^{12}\,\Omega$
Saturation voltage for a $\pm 13\,\text{V}$ supply	$\pm 12\,\text{V}$
Slew rate	$4.8\ \text{V}\,\mu\text{s}^{-1}$
Gain-bandwidth product	3.6 MHz

The op-amp is powered from a $\pm 13\,\text{V}$ supply.

An amplifier has a **variable** voltage gain. The minimum voltage gain is 0 and the maximum voltage gain is -60.

(a) Complete the circuit diagram for a voltage amplifier with this specification. [3] 2



Examiner only

(b) (i) Calculate the **two** resistance values which give a maximum voltage gain of –60. Identify the feedback resistance. [2] 2

RF = 60k -60/1 = -60

R IN = 1k

(ii) What is the input impedance of this voltage amplifier? [1] 1

1k (R IN)

(c) The voltage gain is adjusted and the output voltage measured to be –9 V when the input voltage is 200 mV. Calculate the new voltage gain. [1] 1

-9 / 200m = -45 v

(d) The voltage gain is changed to –30. Calculate the maximum bandwidth of the amplifier with this voltage gain. [2] 2

3.6M / 30 = 120k Hz

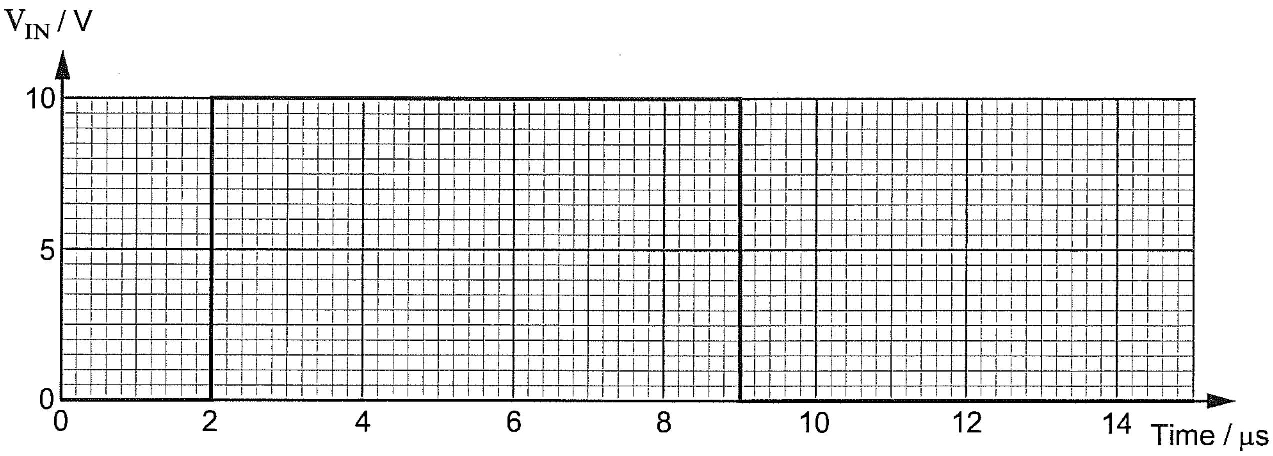
TURN OVER FOR THE REST OF THE QUESTION.

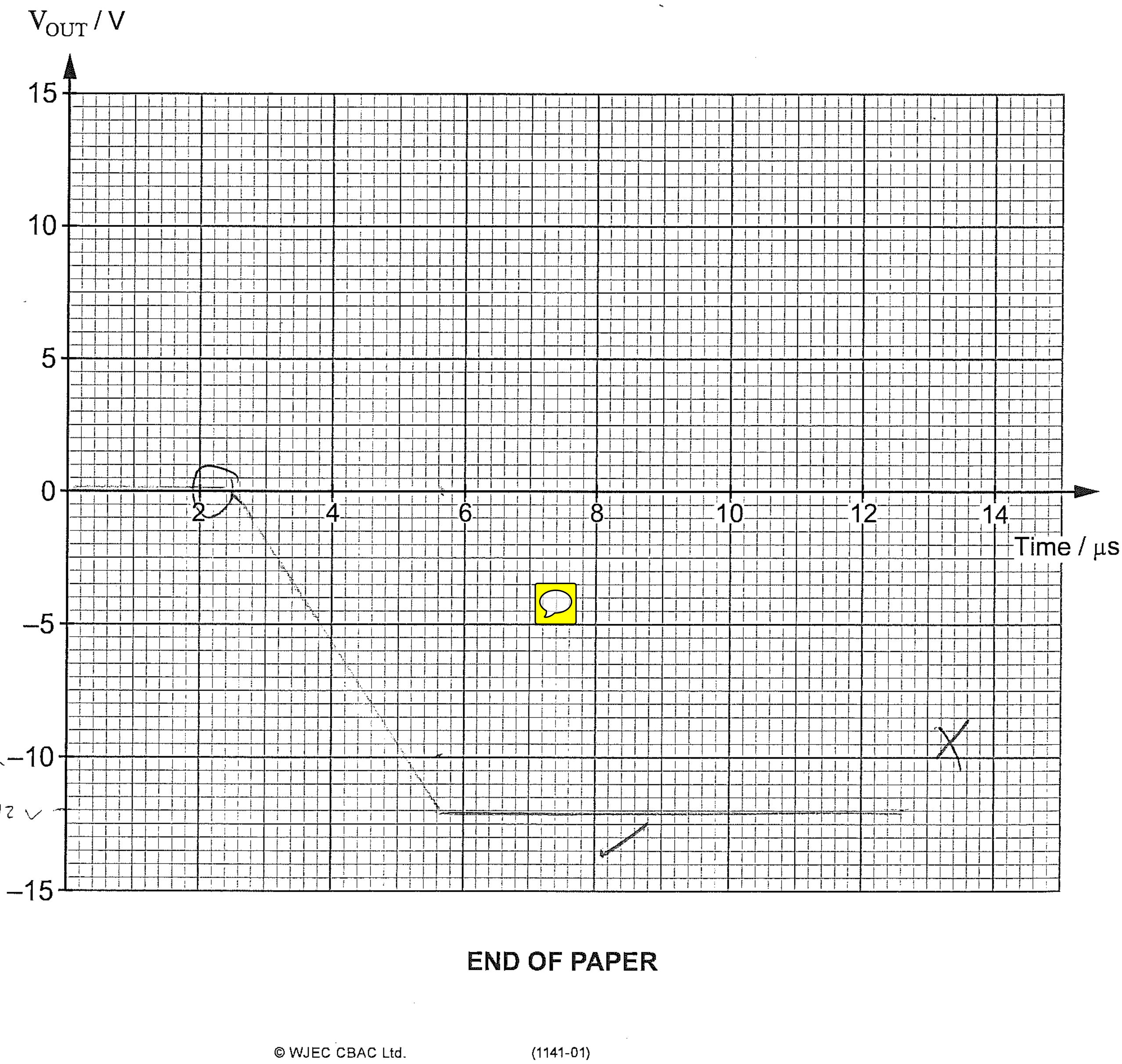
Examiner only

(e) The following signal is applied to the input to illustrate the effect of slew-rate on the output of the voltage amplifier.

Draw the output voltage on the axes below. V_{OUT} **is initially at 0 V.** [3]

1





Saturation voltage ±12 V

END OF PAPER

9

Examiner only

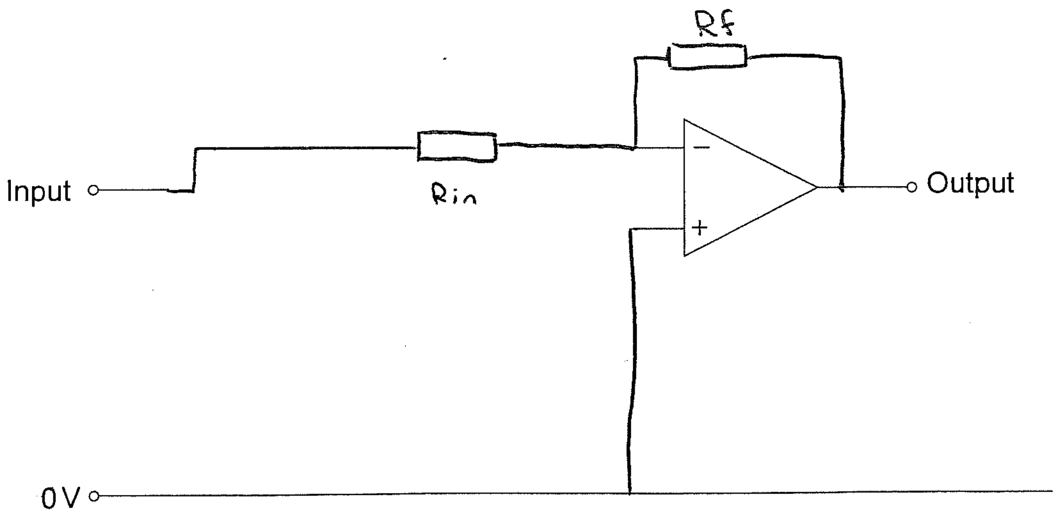
8. A data sheet for an op-amp is given below.

Parameter	**Value**
Open-loop gain	3.0×10^5
Input impedance	$2.0 \times 10^{12}\,\Omega$
Saturation voltage for a $\pm$ 13 V supply	$\pm$12 V
Slew rate	4.8 V μs^{-1}
Gain-bandwidth product	3.6 MHz

The op-amp is powered from a $\pm$13 V supply.

An amplifier has a **variable** voltage gain. The minimum voltage gain is 0 and the maximum voltage gain is -60. inverting

(a) Complete the circuit diagram for a voltage amplifier with this specification. [3]



Examiner only

(b) (i) Calculate the **two** resistance values which give a maximum voltage gain of −60. Identify the feedback resistance. [2]

$G = -\frac{R_F}{R_{in}} = \frac{60}{1} = 60 = -60$

$R_{in} = 1 K\Omega$

$R_F = 60 k\Omega$ feedback resistance

(ii) What is the input impedance of this voltage amplifier? [1]

$1 k\Omega$

(c) The voltage gain is adjusted and the output voltage measured to be −9 V when the input voltage is 200 mV. Calculate the new voltage gain. [1]

$200 mV = 0.2 V \quad \frac{9V}{0.2V} = 45 = -45$

(d) The voltage gain is changed to −30. Calculate the maximum bandwidth of the amplifier with this voltage gain. [2]

$BW = \frac{GBWP}{G} = \frac{3.6 \times 10^6}{30} = 120.000 Hz$

$= 120 \; kHz$

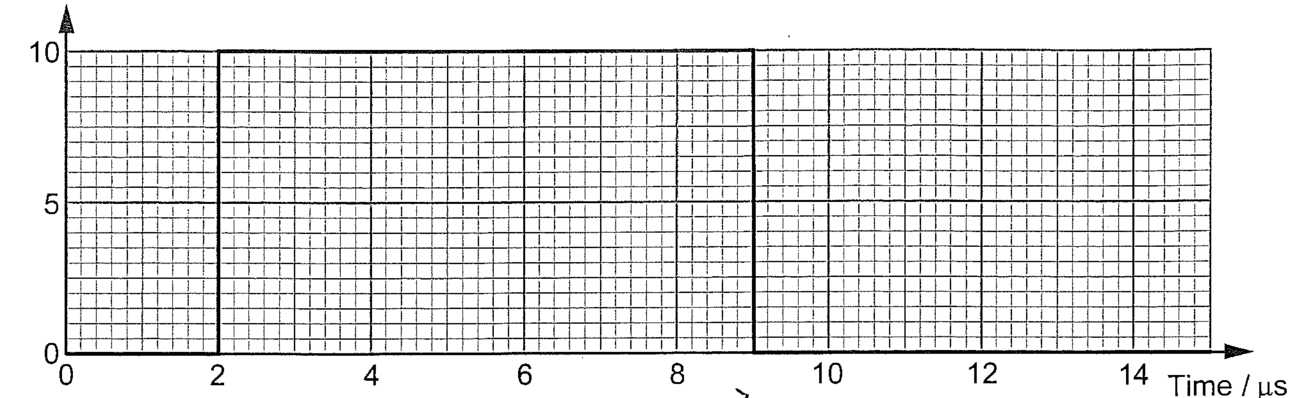
TURN OVER FOR THE REST OF THE QUESTION.

Examiner only

(e) The following signal is applied to the input to illustrate the effect of slew-rate on the output of the voltage amplifier.

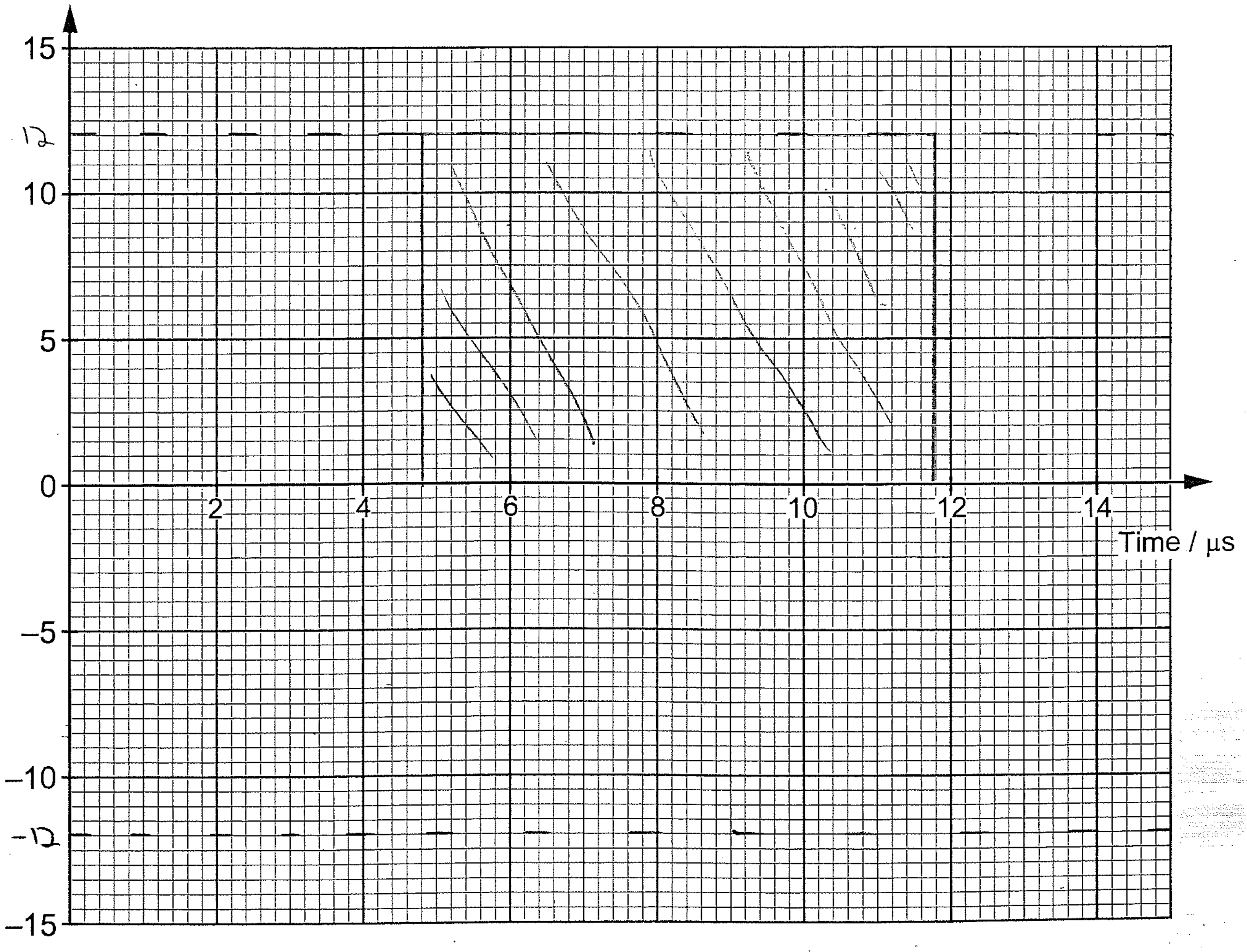
Draw the output voltage on the axes below. V_{OUT} **is initially at 0 V.** [3]

slew rate $= \frac{V_{out}}{t} = \frac{V_{out}}{7}$



7 μs

saturation ±12V



END OF PAPER

Examiner only

8. A data sheet for an op-amp is given below.

Parameter	**Value**
Open-loop gain	3.0×10^5
Input impedance	$2.0 \times 10^{12}\,\Omega$
Saturation voltage for a $\pm 13\,V$ supply	$\pm 12\,V$
Slew rate	$4.8\ V\,\mu s^{-1}$
Gain-bandwidth product	3.6 MHz

The op-amp is powered from a $\pm 13\,V$ supply.

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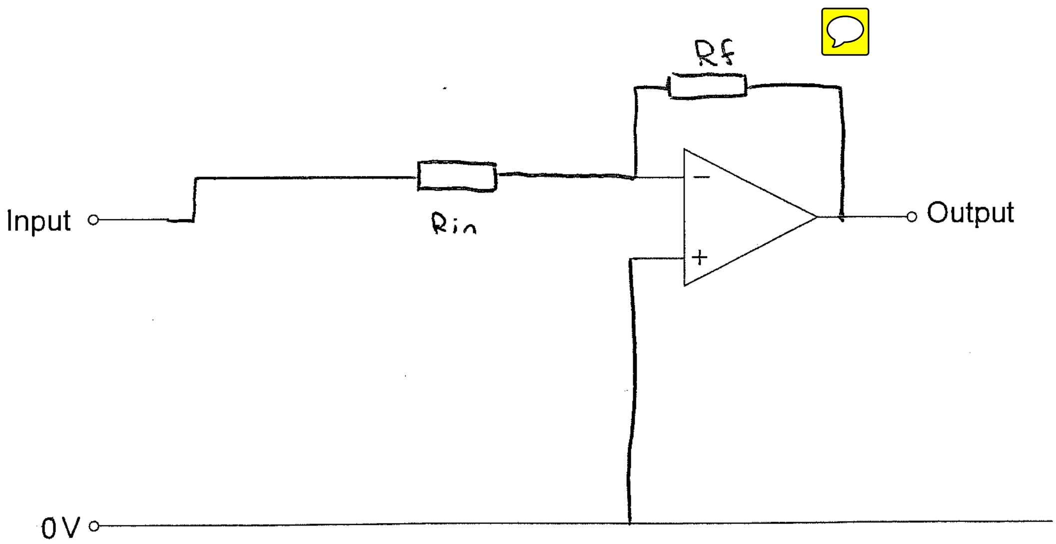

Examiner only

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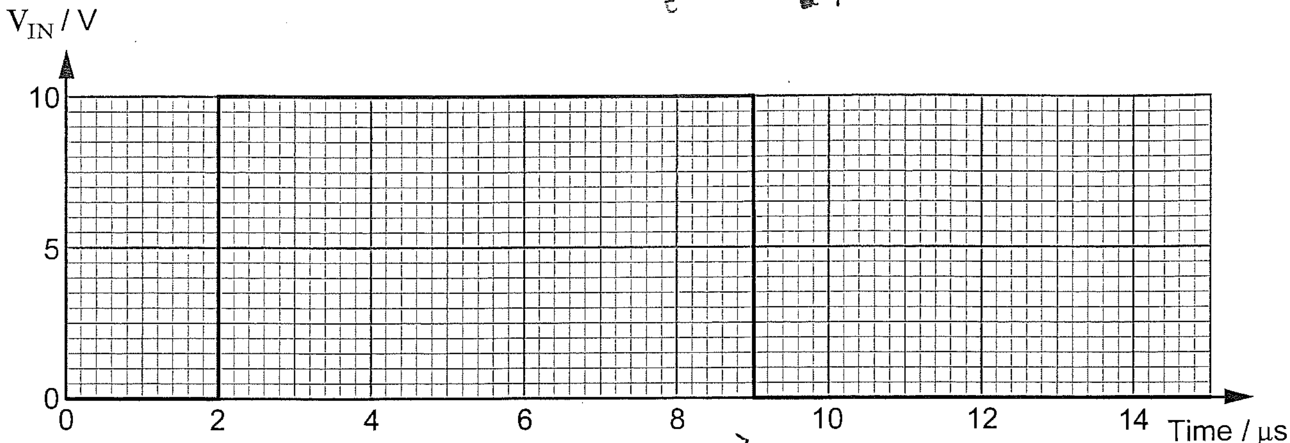

7 μs

saturation ±12V

END OF PAPER